IN THE CLAIMS:

Applicant proposes to amend claims 1 through 12. Applicant also proposed to add new claims 13 through 15. Please note that all claims currently pending and under consideration in the referenced application are shown below. Applicant requests entry of the proposed amended and new claims as shown below; this listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently Amended) A substrate for testing semiconductor devices, comprising:
a semiconductor substrate having a dielectric layer on an exposed surface thereof;
at least one conductive trace on ~~said~~the dielectric layer;
a passivation layer over ~~said~~the at least one conductive trace and ~~said~~the dielectric layer; and
a metal-lined via in ~~said~~the passivation layer in electrical communication with ~~said~~the at least one conductive trace, wherein ~~said~~the metal-lined via is sized and configured to temporarily ~~receive~~ establish an electrical connection by way of biased contact against a substantially spherical interconnection element attached to a semiconductor device.

2. (Currently Amended) The substrate of claim 1, wherein ~~said~~the metal-lined via is formed of a size and shape to receive approximately 10% to 50% of an overall height of ~~said~~the substantially spherical interconnection element.

3. (Currently Amended) The substrate of claim 2, wherein ~~said~~the metal-lined via is formed of a size and shape to receive approximately 30% of ~~said~~the overall height of ~~said~~the substantially spherical interconnection element.

4. (Currently Amended) The substrate of claim 1, wherein ~~said~~the metal-lined via includes sloped sidewalls.

5. (Withdrawn) The substrate of claim 1, wherein ~~said~~the metal-lined via includes stepped sidewalls.

6. (Currently Amended) The substrate of claim 1, wherein ~~said~~the at least one conductive trace comprises copper.

7. (Currently Amended) The substrate of claim 1, wherein ~~said~~the passivation layer comprises polyimide.

8. (Currently Amended) The substrate of claim 1, wherein ~~said~~the metal-lined via comprises a metal from the group comprising gold, platinum, palladium, and tungsten.

9. (Currently Amended) The substrate of claim 1, wherein ~~said~~the dielectric layer comprises silicon dioxide.

10. (Currently Amended) The substrate of claim 1, wherein ~~said~~the passivation layer has a thickness of about 20 to 25 microns.

11. (Currently Amended) The substrate of claim 1, wherein ~~said~~the passivation layer has a thickness of about 100 microns.

12. (Withdrawn) The substrate of claim 1, further comprising:
at least one additional conductive trace over ~~said~~the passivation layer;
a second passivation layer over ~~said~~the at least one additional conductive trace; and
a second metal-lined via in ~~said~~the second passivation layer in electrical communication with ~~said~~the at least one additional conductive trace.

13. (New) The substrate of claim 1, wherein the metal-lined via is sized and configured to temporarily establish the electrical connection comprising a discrete

interconnection at a contact line at least partially circling the substantially spherical interconnection element.

14. (New) The substrate of claim 13, wherein the metal-lined via is sized and configured to temporarily establish the electrical connection comprising the discrete interconnection at a plurality of contact lines at least partially circling the substantially spherical interconnection element.

15. (New) The substrate of claim 14, wherein the metal-lined via is sized and configured to temporarily establish the electrical connection comprising the discrete interconnection at the plurality of contact lines circling the substantially spherical interconnection element.